Current-mode Winner-take-all circuits

CNS WS08 Class

Giacomo Indiveri
Institute of Neuroinformatics
University of Zurich and ETH Zurich

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Outline

Current-mode circuits

- The Translinear principle
- Current-mode resistive networks
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Current-mode circuits

Historically, analog design has been viewed as a voltage dominated form of signal processing. With the advent of (Bi)CMOS technology, shrinking feature size, and reduction of supply voltage a new class of circuits has been developed: current-mode circuits, in which input, output signals, and state variables are represented by currents.

Examples of classical current-mode circuits include:
- translinear circuits
- current conveyors
- dynamic current mirrors
- switched current integrators
- current-feedback amplifiers

Translinear circuits

The term translinear was coined by Barry Gilbert in 1975. In translinear circuits transistors have a transconductance which is linearly proportional to the output current. This applies to:
- Circuits using monolithic BJTs
- Circuits using subthreshold MOS FETs in saturation

For subthreshold MOSFETs in saturation:

\[
I_{DS} = I_0 e^{(\kappa V_G - V_S)/U_T}
\]

\[
g_m = \frac{d}{dV_G} I_{DS} = \frac{\kappa}{U_T} I_{DS}
\]
The translinear principle

Many current-mode circuits comprise transistors arranged in one or more closed loops of junctions.

\[ I_4 V_4 \lambda_4 V_5 \lambda_5 I_5 \]

In a closed loop containing an even number of forward-biased junctions arranged so that there are an equal number of clockwise-facing and counter clockwise facing polarities, the product of the current densities in the clockwise direction is equal to the product of the current densities in the counter clockwise direction.

Current-Mode Low pass filter circuit

Resistive networks

\[ V_{gs}^{M1} + V_{gs}^{M2} - V_{gs}^{M3} - V_{gs}^{M4} = 0 \]

\[ I_{ds} = I_0 e^{\frac{V_{gs} - V_T}{\tau}} \]

Resistors can be implemented in VLSI using single MOSFETs (but with very small dynamic range) or more complex circuits (such as the transconductance amplifier). But if we consider currents, and not voltages, to represent input and output signals of MOSFETs, then we can implement wide dynamic range resistive networks using single transistors instead of resistors.
**Diffusor and pseudo-conductances**

(K. Boahen and E. Vittoz, late nineties)

A conventional conductance $G$ is defined by the relationship

$$I_{ds} = G (V_s - V_d)$$

If we define $V^* = V_0 e^{-V UT}$ as a pseudo-voltage and $G^* = V_0 e^{\kappa V UT}$ as a pseudo-conductance, then

$$I_{ds} = G^* (V^*_s - V^*_d)$$

But this is equivalent to:

$$I_{ds} = I_0 e^{\kappa V UT} - V_0 UT - I_0 e^{\kappa V UT} - V_d UT$$

The diffusion current $I_3$ through $M_3$ is proportional to $(I_2 - I_1)$. The proportionality factor can be modulated by $V_{ref}$ and $V_3$.

**Current divider**

Currents are conveyed from the input terminal (X or Y) to the output terminal (Z), while decoupling the circuits connected to these terminals.

1. The potential at the output terminal (Z) is independent of the current applied at the node Y.
2. An input current that is forced into node X results in an equal amount of current flowing into node Y.
3. The input current flowing into node X is conveyed to node Z, which has the characteristics of a high output impedance current source.

**Diffusor and resistive networks**

**Diffusion equation**

$$\lambda^2 \frac{d^2}{dx^2} V_{out}(x) = V_{out}(x) - V_{in}(x)$$

$$e^{\kappa V UT} (V_{out} - V_{in}) (I_{outj+1} - 2I_{outj} + I_{outj-1}) = I_{outj} - I_{inj}$$

$$\lambda = e^{\kappa V UT} (V_{out} - V_{in})$$
Subthreshold current conveyor

Exploits subthreshold MOSFETs exponential characteristic.

\[ I_z = I_x \\
V_x \propto \ln(I_y) \]

Used in:
- Low-pass filters
- Multiplier circuits
- Winner take all circuits
- Silicon neurons
- Current-mode silicon retinas

Current conveyor as a multiplier

Exploits the translinear principle:

\[ V_x + (V_y - V_x) + (V_w - V_y) + (0 - V_w) = 0 \]

\[ I_x \cdot I_y \cdot \frac{1}{I_w} \cdot I_z = 1 \]

\[ \Rightarrow I_z = \frac{I_x I_y}{I_w} \]

Current conveyor as a current mirror

As voltages at nodes Y and X are decoupled from each other, X can be clamped to a desired constant by choosing appropriate values of \( I_y \).

Gilbert normalizer

\[ I_{in,1} = I_0 e^{V_{d,1}/V_T} \]

\[ I_{out,1} = I_0 e^{V_{d,1}/V_T} \]

\[ I_b = \sum_j I_{out,j} \]

\[ I_{out,i} = I_b \frac{I_{in,i}}{\sum I_{in,j}} \]
WTA networks

- Networks of competing cells (neural, software, or hardware) that report the response of the cell with the strongest activation while suppressing the responses of all other cells.
- Typically used to implement and model competitive mechanisms among populations of neurons.
- Vast literature dating to the 70s for theoretical models, software algorithms, and analog VLSI implementations.

Current-mode WTA circuit

First condition

\[ I_{in,1} = I_{in,2} = I_{in} \]

\[ I_{out,1} = I_{out,2} = I_{b} / 2 \]

\[ V_{d,1} = V_{d,2} \approx V_{c} + V_{b} \]

\[ V_{c} = \frac{k}{U_{T}} \ln \left( \frac{I_{in}}{I_{0}} \right) \]
Current-mode WTA circuit

Second condition

\[ I_{in,1} \gg I_{in,2} \]

\[ V_C = \frac{k}{\beta} \ln \left( \frac{I_{in,1}}{I_0} \right) \]

\[ V_{d,1} = V_C + V_b \]

\[ V_{d,2} \approx 0 \]

\[ I_{out,1} = I_b; I_{out,2} = 0 \]

WTA circuit measurements

Hysteretic WTA

Third condition

\[ I_{in,2} = I_{in} \]

\[ I_{in,1} = I_{in} + \delta I_{in} \]

\[ I_d = I_{sat} \left( 1 + \frac{V_e}{V_{th}} \right) \]

\[ V_{d,2} = V_{d,1} - \frac{\delta I_{in}}{I_{sat}} \]

\[ I_{out,2} < I_{out,1} \]